REMARKS/ARGUMENTS

The specification has been amended to correct typographical errors introduced during preparation of the application, and to properly reflect the relationship of figures 4 and 5. No new matter has been added.

New claims 100-104 have been added to more clearly define the invention, and are believed to be immediately allowable over the prior art.

With respect to election/restrictions, the Office Action indicates on the attached form PTO 326 that claims 31-65 have been withdrawn from consideration. On Page 2 of the Office Action, at paragraph 1, the Office Action indicates that claims 1-30 and 66-99 have been withdrawn from consideration. In view of the Response to Restriction Requirement filed by the applicant on November 7, 2001 the latter indication is erroneous. Non-elected claims 31-65 have been canceled without prejudice. Accordingly, claims 1-30 and 66-104 are pending in the application.

The Examiner's objection to the figures has been noted, and a copy of figure 4, including proposed changes (shown in red), is submitted herewith for approval by the Examiner.

Claims 1-2, 4-7, 9-30, 66-67, 69-72 and 74-96 stand rejected under 35 U.S.C. § 103(a) has been unpatentable over applicant admitted prior art (AAPA) in view of the "Intel 2000 Packaging Data Book" (Intel). These rejections are traversed, inasmuch as the invention, as claimed, is not taught or suggested by the prior art of record.

The present invention relates to "a method and apparatus for reducing bias voltage drops within a substrate." Page 1, lines 2-3. The invention provides a conductive layer secured to a backside of a semiconductor substrate to help maintain a more uniform level of bias voltage within the substrate. The substrate has electrical elements fabricated on its upper, active side. Page 2, lines 12-13.

Accordingly, claim 1 recites:

> A semiconductor device comprising: a semiconductor substrate; at least one electrical element circuit fabricated on an upper side of said substrate; a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and a conductive layer provided on a back side of said substrate. (Emphasis added).

In contrast, Intel relates to wafer metallization which provides an "ohmic contact to the silicon die for the purpose of substrate biasing for those die attach media that do not readily form an ohmic junction." Paragraph 3.3.1, lines 2-3. Intel discusses substrate metallizations which resist oxidation and " are electrically conductive for those devices that require electrical contact." Paragraph 3.3.1, lines 11-12. The Intel reference goes on to discuss die attach media which provide "a means for making an electrical connection to the die backside for those devices requiring it." Paragraph 3.3.1, lines 17-18. Finally, Intel notes that "some of the devices require an ohmic contact to the die backside." Paragraph 3.3.3.5, line 2.

As indicated by the Examiner in the Office Action, the specification recites that "[i]t is common to provide a substrate bias voltage Vbb via a plurality of well plugs, such as P-well plugs." Such P-well plugs are shown in the substrate at 14 on figure 2, which shows an exemplary embodiment of the invention.

The prior art does not teach or suggest, however, the unique combination of claim elements recited in claim 1, including "a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and a conductive layer provided on a back side of said substrate." The use of P-well plugs within a semiconductor substrate, described as prior art in the application, does not teach or suggest "a plurality of bias voltage distribution regions fabricated over said upper side of said substrate," (emphasis added). Likewise, there is no

teaching or suggestion in Intel of a "plurality of bias voltage distribution regions fabricated over said upper side of said substrate." Accordingly, neither the AAPA nor the Intel reference alone teaches the combination of bias voltage distribution regions over an upper side of a substrate with a conductive layer on a back side of the substrate taught or suggested in the prior art.

In order to properly combine references for purposes of rejecting a claim under 35 U.S.C. § 103(a) a basis must be found in the prior art for making the combination. No such basis exists in the AAPA, the Intel reference, or any other reference now record. Absent hindsight, there is nothing in the prior art of record to teach or suggest the combination of P-well plugs with the disclosure of the Intel reference so as to arrive at the unique invention claimed in the present application.

In view of the foregoing, the rejection of claim 1 under 35 U.S.C. § 102(a) over Intel in view of the instant specification is erroneous, and withdrawal of the rejection is in order.

Claims 2, 4-7 and 9-30 each depend, directly or indirectly from claim 1 and incorporate every limitation thereof. Accordingly, the rejections of claims 2, 4-7 and 9-30 under 35 U.S.C. § 102(a) over AAPA in view of Intel should be withdrawn for the same reasons given above with respect to claim 1.

Claim 66 recites:

> A processor system comprising: a processor; a memory device in electrical communication with said processor; at least one of said memory device and said processor comprising: a semiconductor substrate; at least one electrical element fabricated on an upper side of said substrate; a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and a conductive layer provided on a back side of said substrate. (Emphasis added).

Claim 66 recites the combination of a plurality of bias voltage distribution regions over an upper surface of a substrate and a conductive layer provided on a back side of the substrate. As discussed above with respect to claim 1, the combination of elements is not taught or suggested by the prior art. Accordingly, the rejection of claim 66 under 35 U.S.C. § 103(a) over AAPA in view of Intel is erroneous and should be withdrawn for the reasons given above with respect to claim 1.

Claims 67, 69-72 and 74-95 each depend, directly or indirectly, from claim 66 and incorporate every limitation thereof Accordingly, the rejections of claims 67, 69-72 and 74-95 under 35 U.S.C. § 103(a) over AAPA in view of Intel is erroneous and should be withdrawn for the reasons given above with respect to claim 66.

Claim 96 recites:

> A semiconductor device comprising: a semiconductor substrate; at least one electrical element fabricated on said substrate; and a conductive layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and at least one non-substrate area of said device. (Emphasis added).

Contrary to the assertion of the Office Action, figure 3-1 of Intel does not show "a semiconductor device comprising a substrate, . . . a conductive layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and at least one non-substrate area of said device." If the silver or gold thick film metallization shown in Intel Fig. 3-1 is taken to be "a conductive layer provided on a backside of said substrate" within the meaning of the claim, then that metallization defines the back surface of the device. Consequently, the Alumina cited by the Examiner is beyond the back surface of the device, and is thus not part of the device. Accordingly, the claimed combination of limitations is not taught or suggested in the prior art. Therefore, the

rejection of claim 96 under 35 U.S.C. § 103(a) over AAPA in view of Intel is erroneous and should be withdrawn.

Claims 3, 8, 68, 73, and 97 stand rejected under 35 U.S.C. § 103(a) over AAPA in view of Intel and in further view of United States Patent No. 5,753,958 to Burr et al. (Burr).

As noted above, claims 3 and 8 depend from claim 1 and incorporate every limitation thereof. Burr is offered by the Office Action for its teaching of a "substrate bias source." While acknowledging that AAPA and Intel do not name what electrical source the backside layer should be connected to and exactly how it should be connected, the Office Action notes that Burr "shows a backside contact 'B' with metallic layer '106' on the backside." The Office Action asserts that it would have been made obvious by the packaging considerations of Intel to provide the AAPA with a metallic backside layer, and it would have been obvious to connect the added backside layer to a substrate bias voltage source to attain a control substrate backside biasing, as is referenced by Intel.

However, the addition of Burr to AAPA and Intel does not remedy the deficiency noted above in relation to the rejection of claim 1 under 35 U.S.C. § 103(a). Even assuming, arguendo, that the proposed combination of references was supported by the prior art, which it is not, the combination of AAPA in view of Intel and in further view of Burr does not teach or suggest "a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and a conductive layer provided on a back side of said substrate," as recited in claim 1. Accordingly, the rejections of claims 3 and 8 under 35 U.S.C. § 103(a) over AAPA in view of Intel and in further view of Burr should be withdrawn, and claims 3 and 8 should be allowed to issue.

Claims 68 and 73 depend, directly or indirectly, from claim 66 and incorporate every limitation thereof. As noted above in relation to the rejection of claim 66 under 35 U.S.C. § 103(a) with respect to the combination of AAPA and Intel, the proposed

combination of AAPA and Intel does not teach "a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to said substrate; and a conductive layer provided on a back side of said substrate," (emphasis added). As further noted above with respect to the rejections of claims 3 and 8 under 35 U.S.C. § 103(a) over AAPA in view of Intel and Burr, the Burr reference does not remedy this deficiency. Accordingly, the rejections of claims 68 and 73 under 35 U.S.C. § 103(a) over AAPA in view of Intel and Burr should be withdrawn.

Claim 97 recites:

> A semiconductor device comprising: a semiconductor substrate; at least one electrical element fabricated on an upper side of said substrate; a plurality of bias voltage distribution regions fabricated over said upper side of said substrate for receiving a bias voltage and providing said bias voltage to at least some portion of said substrate; and a conductive layer provided on a backside of said substrate, said conductive layer forming an electrical path between said substrate and said bias voltage source. (Emphasis added).

As discussed above with respect to claims 1 and 66, the combination of "a plurality of bias voltage distribution regions" and "a conductive layer provided on a backside of said substrate" is not taught or suggested by the prior art. As further noted above with respect to the rejections of claims 3 and 8 under 35 U.S.C. § 103(a) over AAPA in view of Intel and Burr, the Burr reference does not remedy this deficiency. Accordingly, the rejection of claim 97 under 35 U.S.C. § 103(a) over AAPA in view of Intel and Burr should be withdrawn.

Claims 98 and 99 stand rejected under 35 U.S.C. § 103(a) over AAPA in view of Intel and in further view of United States Patent No. 6,147,857 to Worley et al. (Worley).

Claims 98 and 99 recite the combination of a plurality of bias voltage distribution regions over an upper surface of a substrate and a conductive metallic layer provided on a back side of the substrate. As discussed above with respect to claims 1, 66 and 97, this combination of elements is not taught or suggested by the prior art. The Worley reference is offered in the Office Action for an optional bypass capacitor that has a back side metal layer acting as a capacitor electrode wherein the backside 311 is wire bonded by bonding wire 310 to pad 309. This addition, however, does not remedy the above-noted deficiencies of the prior art with respect to the instant rejections. Accordingly, the rejections of claims 98 and 99 under 35 U.S.C. § 103(a) over AAPA in view of Intel and Worley should be withdrawn.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned **"Version with markings to show changes made."**

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

Please rewrite the paragraph beginning on page 2, line 3 as follows:

It is known in the art to maintain a stable substrate bias voltage Vbb over a large area of the substrate by spacing the well plugs close together, however this occupies large substrate real estate. It is also known to use a heavily doped substrate[s] with a lightly doped epitaxial layer to help stabilize the substrate voltage; however such processes are expensive. It would be desirable to have a semiconductor device and method of making the same that cost effectively reduces bias voltage Vbb drop across the substrate, and which also reduces the number of P-well plugs required to supply the bias voltage Vbb over a given substrate area.

Please rewrite the paragraph beginning on page 4, last line as follows:

FIG. 5 is [a cross-sectional]<u>an elevation</u> view of FIG. 4 <u>taken at V-V</u>.

Please rewrite the paragraph beginning on page 12, line 19 as follows:

Like the conductive metallic layer described above, if conductive paste 60 is not in direct electrical communication with bonding pad 85, it will still draw unwanted voltage or electrical noise away from substrate 10 to help stabilize the operation of the electrical elements of the device 100. Unwanted voltage noise in substrate 10 may exit the substrate 10 by moving vertically down substrate 10 to conductive paste 60 where it [is] flows through the conductive paste 60. For example, transferred noise in conductive paste 60 may horizontally flow away from gate stacks 40, 42 and re-enter substrate 10 in the proximity of P-well diffusion regions 14. The noise can then flow from P-well diffusion regions 14 to P-well plugs 30. From the P-well plugs 30, the voltage can flow to bonding

pads 83, via metalization layers 90, where it can further flow away from active areas of device 100.

Please rewrite the paragraph beginning on page 17, line 13 as follows:

FIG. 5 is [a cross-sectional]an elevation view of FIG. 4 taken at line V-V. Conductive layer 60 is shown attached to the substrate bottom surface 81 with a conductive adhesive 62. Lead fingers 87 are shown attached to the top surface 91 of device 100 by a conductive adhesive compound 94 using well known lead on chip techniques. Also shown is bonding pad 85 which is in electrical communication with conductive layer 60 via wire bond [82]95.